HYPERVELOCITY IMPACT ON SILICON WAFERS WITH METALLIC AND POLYMERIC COATINGS

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ABSTRACT

Current and near future developments in microsystem technologies (MST, also known as MEMS) are defining a new trend towards lower mass, smaller volume spacecraft, without loss of functionality. The MST spacecraft components are etched onto silicon wafers coated with different metallic or polymeric material layers (typically 1-2 microns in thickness). These silicon wafers are then integrated to provide the spacecraft structure subsystem.

For the majority of spacecraft, small debris and meteoroid impacts are not often able to cause large satellite platform failures, due to the shielding provided by existing structural and thermal materials and the high percentage of 'empty volume' contained within a typical spacecraft structure. Smaller satellites incorporating MST and based on silicon wafers, whilst presenting a smaller surface area, are expected to be vulnerable to impacts as the lower subsystem mass defines a less substantial structure, providing significantly less protection against impact.

This paper presents results of a BNSC-funded study aimed at identifying the vulnerability of MST technologies based on silicon wafers to space debris and meteoroid impact. Hypervelocity impact tests were carried out on silicon wafers coated with five different types of deposited material. Multiple glass spheres were fired simultaneously at velocities in the range of 6 km/s.

The impact results identify the hypervelocity impact response of the silicon wafers. The impacted targets showed a brittle material damage morphology (defined by fracture) and linked to the crystalline structure of the silicon wafer. As predicted from the mechanical properties, it was found that the silicon tended to fracture along the 111 planes. Cross-sectioned craters also showed the crystalline structure of the silicon, with the onset of fracture-driven spall on the rear surface. The metal and polymeric coatings produced diverse damage morphologies, with delamination zones being up to twice the diameter (diameter ~ 1 mm) of the damage area (diameter ~ 0.5 mm). The results indicate that impact on silicon wafers will define a large damage area and failure modes of the coatings are dependent on the material type. The fracture based failure modes suggest that further post-impact crack growth may occur

1. INTRODUCTION

Spacecraft in orbit around the Earth are exposed to hypervelocity impacts from meteoroids and space debris [1]. For unmanned spacecraft, the structure typically provides the primary shielding against hypervelocity impact by space debris and micrometeoroids. Larger unmanned spacecraft typically have primary and secondary structures made from honeycomb (aluminium or carbon fibre reinforced plastic facesheets bonded onto an aluminium core). The impact response of some honeycomb structures, and modifications to improve the shielding performance, has recently been assessed [2].

For smaller satellites, the structural requirements due to launch environment are less than for larger satellites. This means that structural protection afforded against hypervelocity impact decreases. In addition, the miniaturisation of components (by etching them onto coatings deposited onto silicon wafers) means that silicon based components may form part of the primary structure. These components are known as MEMS or MST devices. They may also be externally mounted, e.g. the micropropulsion thrusters described in [3]. Therefore, silicon material may provide the shielding against meteoroid and debris impact. The integrity of the silicon wafer upon which components are mounted is required for nominal satellite operation. These small satellites may be flown singly, or as part of a much larger constellation (e.g. formation flying).

Debris mitigation considerations play an increasingly important part in spacecraft design. End-of-life de-orbit, collision avoidance manoeuvres during orbit and spacecraft reliability during the mission are all related to debris mitigation. Some debris mitigation strategies are discussed in [1], and summarised in [4]. Smaller spacecraft are individually less vulnerable, as the risk of an impact of a particle of diameter n mm is equivalent to exposed area x time spent in orbit (the area-time product). However, without the protection of honeycomb-based structures, they may be more vulnerable to smaller diameter projectiles. Calculations in [4] show that, for a 600 km orbit ~10^5 impacts/m^2/yr of 1 μm in diameter or less, but only ~ 10^3

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detectors in LEO have also showed that short-lived debris streams (particles detected in the range 10-50 μm) can increase the impact risk [5].

Redundancy can be built into a distributed system of many satellites, by factoring in a number of "sacrificial" satellites. However, if these satellites are disabled due to a debris impact, they can then no longer carry out an end-of-life manoeuvre, and will become a risk debris object themselves. Due to the small size of these objects, they may be more difficult to track and the difficulty of carrying out successful collision avoidance manoeuvres increases.

In order to evaluate the debris and meteoroid risk, hypervelocity impact (HVI) testing must be carried out to establish damage morphology and potential failure modes for silicon wafers and coating layers, upon which micro-components will be etched. Post-impact, other space environment driven effects (such as thermal cycling) may act in a synergistic manner to increase the range of the damage caused by the impact.

Only a small number of hypervelocity impact studies on silicon wafers, germanium wafers, polycrystalline diamond deposited on silicon wafers and metal-oxide-silicon (MOS) capacitors based on silicon wafers, have been carried out [6, 7, 8].

This paper presents the results of a hypervelocity impact programme onto silicon wafers, coated with four different types of metallic or polymeric coatings. The damage morphology for impacts onto silicon has been established and is clearly influenced by the crystalline structure. The crater morphology (plan view and cross-section) is driven by failure along the {111} plane. The crater diameter is approximately 10 x projectile diameter. Coating materials deposited on the silicon wafer are delaminated or torn by the impact, increasing the damage diameter up to 20 x projectile diameter. Cracks propagate from the impact site; these may extend under thermal stresses due to space environment effects or component heat generation. Space debris and meteoroid hypervelocity impact effects should be considered in silicon-based component selection and design.

2. MATERIALS AND METHODS

Hypervelocity impact testing was carried out at the University of Kent at Canterbury's Light Gas Gun facility [10]. Multiple soda lime glass spherical projectiles (50 ± 1.2 μm) were fired at the same time (the "buckshot" technique) with impact velocities being recorded in the range between 5.5 and 5.9 km/s. The hypervelocity impact programme was designed to obtain a first indication as to the response of silicon wafers (with a number of types of deposited layers, the "coatings") under hypervelocity impact, and to obtain the large numbers of impact data, for a statistical analysis of crater diameter. Four different target types were tested; one shot was repeated twice (onto two during the first test. A benefit of the sabot fragment impact was that it caused significant fracturing and, as a result, cross-sectioned craters caused by hypervelocity impact of the projectiles. Limitations of the test programme include the relatively low impact velocity, compared with simulation predictions [4], and the size of the impacting projectile compared with the coating thicknesses (in the range 1-10 μm). Having evaluated the impact response of the silicon wafer, further shot programmes will evaluate the target response using smaller diameter projectiles.

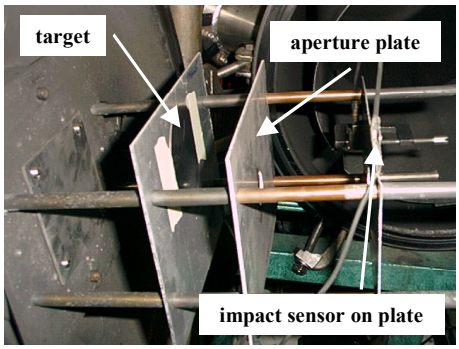


Fig. 1. Experimental Configuration

All wafers were created using standard semiconductor wafer processing techniques. These techniques were originally developed for the semiconductor "chip" manufacturing industry and have been modified to handle thicker films that are useful in creating MST type devices. These types of devices might be expected to appear on the exterior of small satellites in the form of micro-thrusters, sun sensors, etc.

In all cases the substrate is a standard 3" (76.2 mm) silicon wafer with a crystallographic orientation of 100, and a thickness of 14-16 mils (0.36-0.41 mm). Coatings were produced as described and, unless otherwise stated, the thickness was measured using a standard step-profilometer. The silicon wafer was manufactured by the Polishing Corp of America, the SU8-5 by MicroChem Corp and the polyimide (and polyimide developer) by OCG Microelectronic Materials.

Si+polyimide (Target MST-Si-02). The polyimide was pored and spun on at 3000 RPM for 30 sec. The wafer was subsequently baked for 1hr at 90 degrees C. It was then exposed using a standard UV bulb photo aligner and a quartz photomask. The pattern in the polyimide was developed using a developer.

Si+polysilicon (Target MST-Si-03). A thermal Silicon oxide layer was grown on the wafer by placing it in a furnace with oxygen flow. The thickness was measured using a NanoSpec spectrometer. The wafer was returned to a second furnace, where silane was flown over the wafer to grow a poly-crystalline layer of silicon. The wafer was then coated with a standard photo-resist (another photo reactive polymer) and spun at 5000 RPM. The wafer was baked for 1 hr at 90

degrees C. It was then exposed using a standard UV bulb photo aligner and a quartz photomask. The patterned was developed in the photo-resist and the wafer was transferred to a reactive ion etcher (RIE). In the RIE, a sulphur hexafluoride gas plasma etched away any exposed Poly-Silicon stopping at the Oxide layer. The photo-resist was removed in acetone leaving the patterned poly-Silicon stripes. These types of layers are often used in the creation of MST devices and can be purchased from foundries specializing in the production of MST devices on demand

Si+ Ti/Pt/Au (Target MST-Si-04). The wafer was then coated with a standard photo-resist (another photo reactive polymer) and spun at 5000 RPM. The wafer was baked for 1 hr at 90 degrees C. It was then exposed using a standard UV bulb photo aligner and a quartz photomask. The patterned in the photo-resist was developed using a KOH based developer and the wafer was transferred to an electron beam evaporator. The metals were deposited to create a film of conductor on the wafer. The wafer was subsequently transferred to an acetone bath nested into an ultrasonic cleaner. The photo-resist was dissolved and lifted off the metal on top. In this case, only the areas where the photo-resist was removed during patterning will have metallisation left intact. Although the metal types and thickness may very somewhat this is a standard means for forming electrical contacts both in semiconductor chip manufacturing and in MST processing.

Si+Su8 (Target MST-Si-05). The SU8-5 was poured on the wafer and the wafer was spun at 500 RPS for 30 sec, producing a layer 5 um thick. The wafer was subsequently baked for 6 hours at 90 degrees C. This material is photo-reactive and so exposing and developing out the pattern can make fine structures.

Table 1. Target description, shot programme and crater count. V: video imaging; SEM: scanning electron microscope. Numbering format is MST-Si-targetID-shotnumber

Shot ID	Coating	Number of craters imaged
MST-Si-04-01	1.35 μm Ti/Pt/Au	4(V) 6(SEM)
MST-Si-03-02	3 μm SiO2 + 1 μm Polysilicon	37(V) 9(SEM)
MST-Si-05-03	5 μm Su8	30(V) 0(SEM)
MST-Si-02-04	10 μm polyimide	0(V) 3(SEM)
MST-Si-02-05	10 μm polyimide	62(V) 5(SEM)

The targets were imaged using a microscope and video imaging system (Table 1). Scanning electron microscopy (SEM) BEI (back scattered electron imagery) was used for non-metallic coatings on the silicon wafer targets and SEI (secondary electron imagery) and was used for metallic coatings. The target morphology was identified and analysed and the crater dimensions measured in x and y directions. The geometric mean (sqrt(xy)) was taken to produce the average crater diameter. The damage morphology and failure modes are reported in this paper. For three targets (MST-Si-03-02. MST-Si-05-03, MST-Si-02-05), the number of times a particular morphology was noted was recorded. Analysis of the characteristic fracture angles was carried out and the crater morphology compared with impacts on soda-lime glass.

3. RESULTS

As the impacting particle diameter was much greater than the thickness of the deposited layers, the silicon wafer was exposed as a result of the impact process. For some wafers with etched patterns, the silicon wafer (+SiO2, where applicable) was exposed prior to impact. General silicon cratering morphologies were observed on all targets. The results reported are also applicable to the Si+polysilicon target. Retained platelets (64-76% of targets), parallel features on opposing sides (60-65%) (both shown in Fig. 2) were observed on all target types using video imaging. Parallel sided craters (53-70%) and right-angled features (49-67%) (Fig. 3). The crater interior was imaged using the SEM – a cross-shaped fracture-based feature (Fig. 4) (called a “Maltese cross”, due to the valley shaped arms – shown in greater detail in Fig. 5). The crater interiors appear to be divided into a number of concentric regions, broadly divided into two zones. The outer zone (Fig. 6) includes the arms of the Maltese cross and is generally radial in nature. The radial pattern is abruptly disrupted and is replaced by a smoother surface with ripple marking (Fig. 7); this boundary marking a sharp change in crater wall gradient. The inner zone (Fig. 6) includes crushed silicon fragments with random orientation (higher magnification image in Fig. 8). Moving away from the centre of the crater, the fragments become larger.

Five cross-sectioned craters were imaged; Fig. 9 represents the typical morphology. The crater has a flat-based shape with steep sides. The steep sides lead to a shallow, near-level zone before reach the wafer surface. This may correlate to the change in gradient and morphology noted above. Horizontal cracks are present, as are step-like planes. Below the crater surface, linear fracture features are observed. These are discussed further in the next section. The rear of a crater was photographed, showing a square feature (Fig. 10), indicative of a square-based pyramid. This is consistent with the crater profile observed in the cross-section and represents the onset of rear spallation (at a particle diameter: target thickness, dp/T = 0.12-0.14).

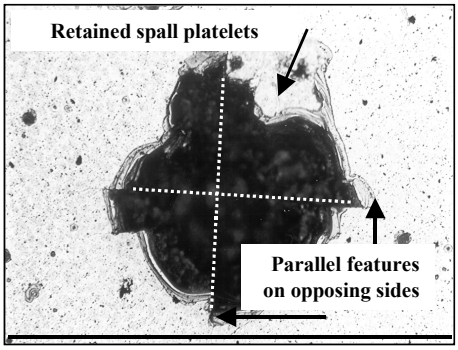
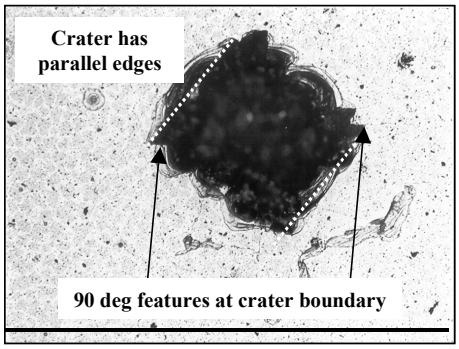


Fig. 2. Impact onto silicon + polysilicon. Scale bar is 1 mm



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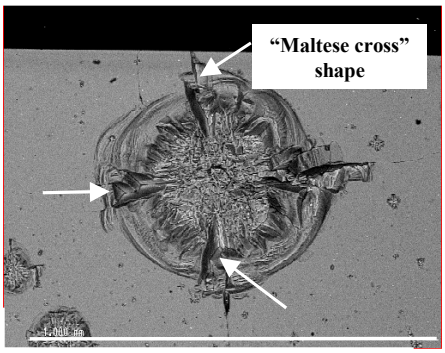

Fig. 4. Impact on exposed Si surface. Scale bar is 1 mm

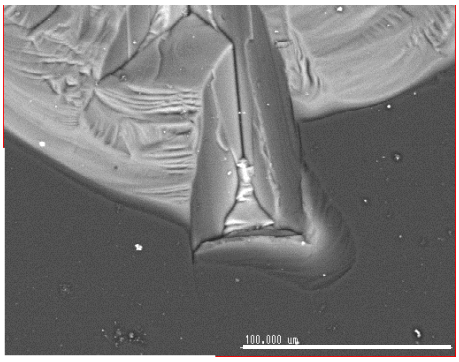

Fig. 5. Valley shaped arms

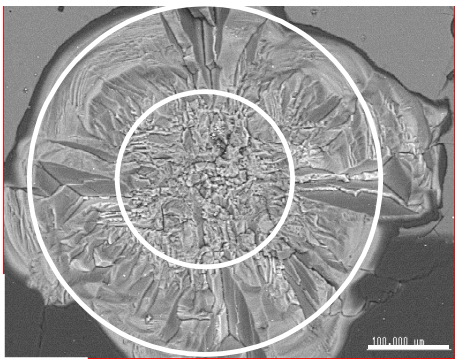

Fig. 6. Inner and outer zone of crater in silicon. Scale bar is 100 microns

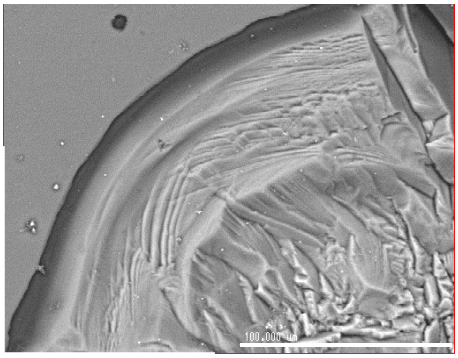

Fig. 7. Shallow ripple effect at crater edge. Scale bar is 100 microns

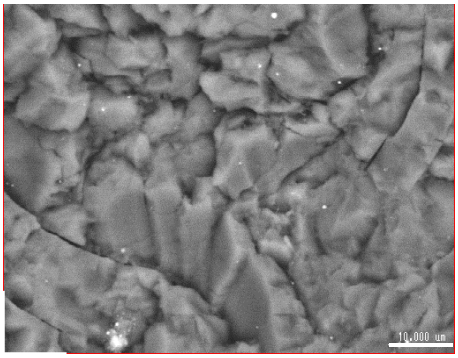

Fig. 8. Silicon morphology at crater centre. Scale bar is 10 microns

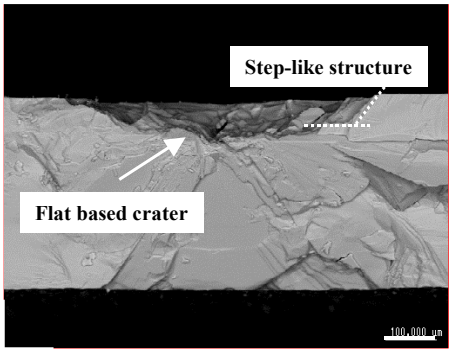

Fig. 9. Crater cross-section. Scale bar is 100 microns

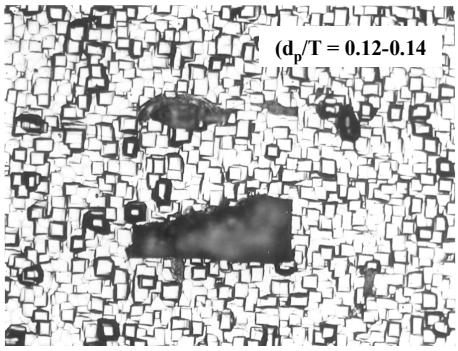

Fig. 10. Rear side damage

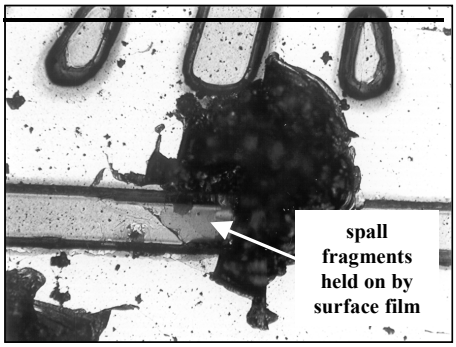

Fig. 11. Polyimide damage. Scale bar is 1 mm

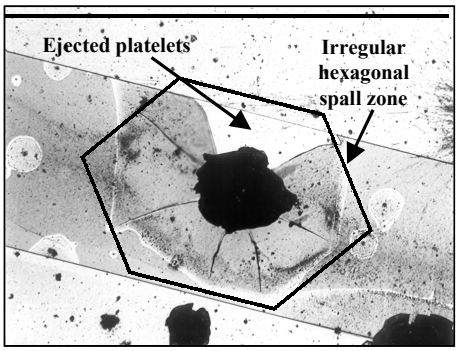

Fig. 12. Si+Su8 damage. Scale bar is 2 mm

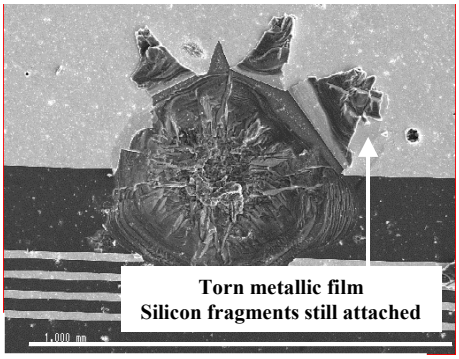

Fig. 13. Au/Ti/Pt damage. Scale bar is 1 mm

For impacts on the Si+polyimide targets (example shown in Fig. 11), a number of features were apparent. For impacts adjacent to a polyimide deposited layer, the crater undercut the polyimide (66%) and the silicon fragments remained attached to the polyimide (38%). For impacts into the polyimide layer (not near a material boundary), the material is crazed and cracked around the impact site (60%), and may be retained and hang into the crater volume (72%).

For impacts on the Si+Su8 targets (example shown in Fig. 12), the impact crater was typically surrounded by irregular hexagonal spall zone (the Su8 polymer film divided into six petalloid segments, each bounded by radial cracks) (occuring for 59% of impacts). Spall fragments were ejected at Su8/Si boundaries (44%) or at hexagonal edge (70%) and retained Su8 segments raised out of plane of the wafer (67%). For a limited number of impacts, the spall zone was completed ejected (15%).

For impacts on the Si+Au/Ti/Pt (Fig. 13), the crater was surrounded by torn fragments of metallic film. The metallic film peel back sometimes extended beyond the crater edge and Si fragments were sometimes still attached. These features were observed on all of the craters imaged.

The mean crater diameters are given in Table 2 (based on the mean of the craters measured in Table 1). The Dcrater values are identical within the error ranges.

Table 2. Mean crater diameters. (The Si+polyimide data is from target MST-Si-02-05.)

Target type	Dcrater (mm)	Velocity (km/s)
Si + Su8	0.50 ± 0.11	5.54 ± 0.25
Si + Au/Ti/Pt	0.44 ± 0.08	5.86 ± 0.25
Si + Polysi	0.59 ± 0.09	5.73 ± 0.25
Si + polyimide	0.56 ± 0.10	5.89 ± 0.25

4. DISCUSSION

Silicon is a crystalline material with a highly ordered lattice structure. Bonding in silicon is highly covalent with a very small degree of ionic nature. Silicon is therefore strong and wear-resistant. However, silicon is a brittle material, and will undergo negligible plastic deformation before failing due to brittle fracture. As silicon is anisotropic, it will fracture preferentially along particular crystallographic planes. Some silicon material properties (Young's modulus, E; Poisson's ratio, ν; Critical stress intensity factor, K1c; Shear modulus, G; Bulk modulus etc) are summarised in Table 3. The data are taken from [11].

Table 3. Silicon material data

	Plane		
Parameter	{111}	{100}	{110}
E (GPa)	172, 169, 187, 188	130	169
ν	0.18, 0.28, 0.45	0.28	0.28
K_{1c} (MPa $m^{½}$)	0.82	0.95	0.95
γ_{hkl} (J m^{-2})	1.23	2.13	1.51
G (GPa)	49 (bulk value)		
B (GPa) at rtp	97.8-98.7 (bulk value)		
ρ (25C)	2.32		

This type of orientation-dependent behaviour can be held responsible for many of the morphological features discussed in the previous section. The failure along particular crystallographic planes is particularly evident in the 'Maltese cross' shape and other perpendicular structures visible in the plan-view images. Also, the cross sections displayed the orientation of the preferred fracture planes with respect to the wafer surfaces, which are known to be {100} planes.

The material fracture data for Si indicate that the material should cleave on its {111}-type planes. A projection of {111} planes onto a (100) surface (i.e. a plan view of the wafer) shows 90° angles at all the points where the planes intercept (Fig 14). This angle, or very close to it, is observed in many of the crater images presented in this paper.

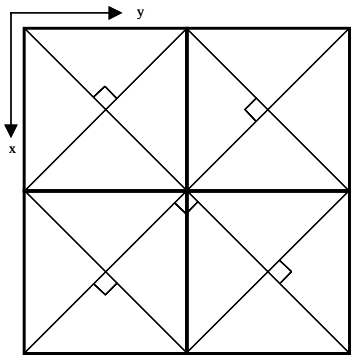

Fig. 14. Projection of {111} planes onto a (100) surface

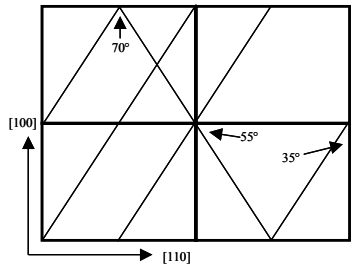

Fig. 15. Projection of {111} planes onto the (110) surface

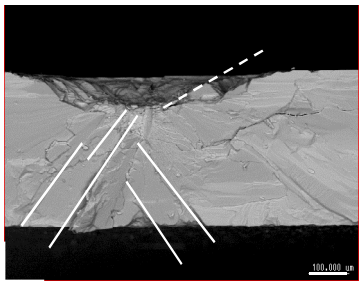

Fig. 16. Scale bar is 100 μm.

A projection of the {111} planes onto the (110) surface (cross-section of crater) identify characteristic angles of 55° and 35° (Fig 15). The images of the cross sections confirm that the material is fracturing along {111} wafer surface (001) is constant at approximately 55°, as shown in Fig. 16 (solid lines). The cracks running at ~35° (dotted lines) are also {111} planes, since they are at 55° to the vertical, (100), which is equivalent in the lattice to (001). These angles are seen both in the deformation underneath the crater and in the walls of the crater itself.

Hence the Maltese cross shape, seen in virtually all of the craters, can be described by a series of intersecting {111} planes along which the silicon has been detached from the rest of the wafer and then ejected. It is also found that all the craters on each wafer are aligned – the arms of the Maltese cross lie in the same directions. The orientation of the craters with respect to the crystal lattice can therefore be deduced, and is shown in Fig. 17. The valley-shaped arms are formed by three {111} planes (denoted by A, B, C in Fig. 18). The apparent narrowing of the arms towards the centre of the crater (making the cross 'Maltese') is caused by the height of the valley sides getting lower towards the centre. In other words, it is not really a projection on (001) but on a plane tilting towards the crater centre. The angle between the valley walls is 70.5°.

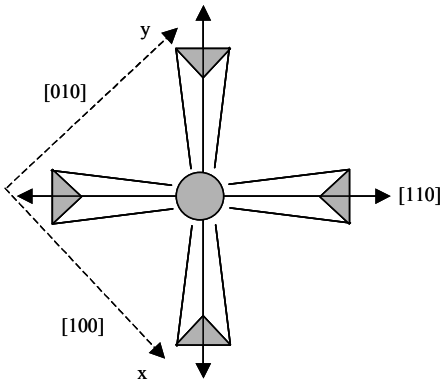

Fig .17. Orientation of Maltese Cross with respect to the silicon lattice. (Projection on (001))

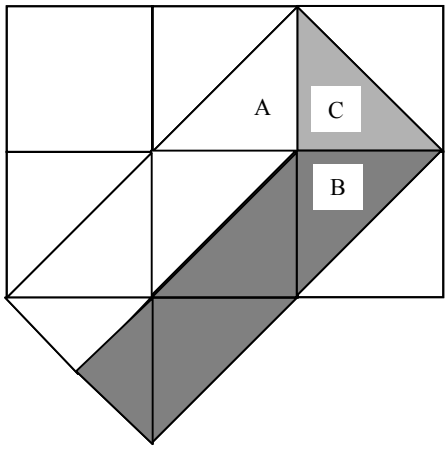

Fig. 18. Plan view of intersecting {111} planes -

5. CONCLUSIONS

This paper presents results identifying the vulnerability of MST technologies based on silicon wafers to space debris and meteoroid impact. Hypervelocity impact tests were carried out on silicon wafers coated with five different types of deposited material, upon which MST components may be etched. Multiple glass spheres were fired simultaneously at velocities in the range of 6 km/s.

The silicon substrate of the targets showed a brittle material damage morphology (defined by fracture), which was linked to the crystalline structure of the silicon wafer. As predicted from the mechanical properties, it was found that the silicon tended to fracture along the 111 planes. Cross-sectioned craters also showed the crystalline structure of the silicon, with the onset of fracture-driven spall on the rear surface. The metal and polymeric coatings produced diverse damage morphologies, with delamination zones being up to twice the diameter (diameter ~ 1 mm) of the damage area (diameter ~ 0.5 mm). The results indicate that impact on silicon wafers will define a large damage area and failure modes of the coatings are dependent on the material type. The fracture-based failure modes suggest that further post-impact crack growth may occur. Further work will include higher velocity, smaller diameter impact tests to investigate more directly impact damage on components etched on the coatings.

6. ACKNOWLEDGEMENTS

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